CLAIMS:

1. A computer system for transferring data to a peripheral device, the computer system comprising:

a CPU;

a first memory that may be written to or read by the CPU;

a second memory that may be written to or read by the CPU; and

a DMA controller coupled with the CPU and the second memory, the DMA controller being operable to:

read data from the second memory and transfer the data to the peripheral device,

create a wait state to prevent the CPU from accessing the second memory while the DMA controller is reading data from the second memory,

enable the CPU to regain access to the second memory once the DMA controller has finished reading data from the second memory, and

allow the CPU to access the first memory without delay even while the DMA controller is reading data from the second memory.

2. The computer system as set forth in claim 1, wherein the DMA controller creates the wait state by suppressing a clock of the CPU while the DMA controller is reading data from the second memory.

3. The computer system as set forth in claim 1, the peripheral device including a display controller and a display.

4. The computer system as set forth in claim 1, further including a selector coupled between an address line of the second memory and the CPU and the DMA controller, the selector being controlled by the DMA controller to connect either the CPU or the DMA controller to the address line.

5. The computer system as set forth in claim 1, further including:

a data bus for transferring data between the CPU and the first memory and the second memory; and

a data bus isolation gate for isolating data lines of the second memory device from the CPU when the DMA controller is reading data from the second memory.

6. The computer system as set forth in claim 1, further including a selector coupled between the CPU and a read/write line of the second memory, the selector being controlled by the DMA controller to force the second memory to a read state when the DMA controller is reading data from the second memory.

7. The computer system as set forth in claim 3, the CPU, the second memory, the DMA controller, and the display controller being integrated on a single chip.

8. The computer system as set forth in claim 1, wherein the first memory and the second memory are formed on separate blocks of RAM.

9. The computer system as set forth in claim 1, wherein the first memory and the second memory are formed on a single block of RAM that is partitioned into first and second portions.

10. A GPS receiver comprising:

an antenna for receiving GPS signals from a plurality of GPS satellites;

a CPU coupled with the antenna for processing the GPS signals to determine location information for the GPS receiver;

a display coupled with the CPU for displaying at least a portion of the location information;

a first memory that may be written to or read by the CPU;

a second memory that may be written to or read by the CPU; and

a DMA controller coupled with the CPU and the second memory, the DMA controller being operable to:

read data from the second memory and transfer the data to the display,

create a wait state to prevent the CPU from accessing the second memory while the DMA controller is reading data from the second memory,

enable the CPU to regain access to the second memory once the DMA controller has finished reading data from the second memory, and

allow the CPU to access the first memory without delay even while the DMA controller is reading data from the second memory.

11. The GPS receiver as set for in claim 10, wherein the DMA controller creates the wait state by suppressing a clock of the CPU while the DMA controller is reading data from the second memory.

12. The GPS receiver as set forth in claim 10, further including a selector coupled between an address line of the second memory and the CPU and the DMA controller, the selector being controlled by the DMA controller to connect either the CPU or the DMA controller to the address line.

13. The GPS receiver as set forth in claim 10, further including:

a data bus for transferring data between the CPU and the first memory and the second memory; and

a data bus isolation gate for isolating data lines of the second memory device from the CPU when the DMA controller is reading data from the second memory.

14. The GPS receiver as set forth in claim 10, further including a selector coupled between the CPU and a read/write line of the second memory, the selector being controlled by the DMA controller to force the second memory to a read state when the DMA controller is reading data from the second memory.

15. The GPS receiver as set forth in claim 10, further including a display controller for driving the display.

16. The GPS receiver as set forth in claim 15, the CPU, the second memory, the DMA controller, and the display controller being integrated on a single chip.

17. The GPS receiver as set forth in claim 10, wherein the first memory and the second memory are formed on separate blocks of RAM.

18. The GPS receiver as set forth in claim 10, wherein the first memory and the second memory are formed on a single block of RAM that is partitioned into first and second portions.